What is claimed is:

1. A semiconductor device having an embedded array, said embedded array having basic cells arranged in a matrix, wherein a basic cell has an impurity region part of which is removed, said part corresponding with a missing contact hole.

2. A semiconductor device according to claim 1, wherein said impurity region is part of a transistor.

3. A semiconductor device according to claim 1, wherein said impurity region is used for applying a substrate bias potential.

4. A semiconductor device having an embedded array, said embedded array having basic cells arranged in a matrix, wherein a basic cell has a gate part of which is removed, said part corresponding with a missing contact hole.

5. A method of designing and manufacturing a semiconductor integrated circuit having an embedded array, said embedded array having basic cells arranged in a matrix, said method comprising the step of, in a design stage, modifying layout pattern data of said embedded array by detecting and removing a non-use area in a basic cell based on layout data of contact holes.

6. A method according to claim 5, wherein said contact holes are for connection between an impurity region of transistors and a line thereover, said step comprises:

segmenting a pattern of said impurity region into

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individual segmentation patterns each as a removal unit, each segmentation pattern corresponding with one or more of all individual contact hole patterns that can be arranged; and

judging one of said removal units as said non-use area if an individual contact hole pattern corresponding with said one of said removal unit is not existent.

7. A method according to claim 6, wherein a pattern of said impurity region includes an area corresponding with a gate, said step further comprises:

obtaining an OR pattern, as a synthesized removal pattern, between a pattern of said gate and said non-use area; and

performing said modifying by removing said synthesized removal pattern from said pattern of said impurity region.

8. A method according to claim 7, wherein said modifying is performed by operating an exclusive OR between said pattern of said impurity region and said synthesized removal pattern.

9. A method according to claim 6, wherein said one or more individual contact hole patterns are those in line along a direction traversing a gate pattern.

10. A method according to claim 6, wherein said one or more individual contact hole patterns is one individual contact hole pattern, and an area of said removal unit

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excludes a close area to a gate.

11. A method according to claim 5, wherein said contact holes are for connection between an impurity region and a line thereover having a substrate bias potential, said step comprises:

segmenting a pattern of said impurity region into individual segmentation patterns each as a removal unit, each segmentation pattern corresponding with one of all individual contact hole patterns that can be arranged; and

judging one of said removal units as said non-use area if an individual contact hole pattern corresponding with said one of said removal unit is not existent.

12. A method according to claim 5, wherein said contact holes are for connection between a gate of a transistor and a line thereover,

segmenting a pattern of said gate into individual segmentation patterns each as a removal unit, each segmentation pattern corresponding with one of all individual contact hole patterns that can be arranged; and

judging one of said removal units as said non-use area if an individual contact hole pattern corresponding with said one of said removal unit is not existent.

13. A method according to claim 12, wherein said individual segmentation patterns have one that is a member of a single transistor assumed to exist; and

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judging said one of said individual segmentation patterns as said non-use area if said single transistor is not existent.

14. A method of manufacturing a semiconductor integrated circuit having an embedded array, said embedded array having basic cells arranged in a matrix, said method comprising the steps of:

designing and manufacturing a prototype of said semiconductor integrated circuit;

performing a test on whether or not an electrical behavior of said prototype meets required specifications;

modifying layout pattern data of said embedded array, if said behavior meets said required specifications, by detecting and removing a non-use area in a basic cell based on layout data of contact holes;

preparing a mask having a modified layout; and

manufacturing a semiconductor integrated circuit from which a non-use area is removed by substituting said mask having said modified layout for a mask before modification.

15. A computer readable storage medium, having thereon computer program to modify layout pattern of an embedded array in a semiconductor integrated circuit, in which basic cells are arranged in a matrix, by detecting and removing a non-use area of a basic cell based on layout data of contact holes.

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16. A storage medium according to claim 15, wherein said contact holes are for connection between an impurity region of transistors and a line thereover, said program comprises the step of:

segmenting a pattern of said impurity region into individual segmentation patterns each as a removal unit, each segmentation pattern corresponding with one or more of all individual contact hole patterns that can be arranged; and

judging one of said removal units as said non-use area if an individual contact hole pattern corresponding with said one of said removal unit is not existent.

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